IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Canceled).

Claim 2 (Currently Amended): A matrix array substrate comprising:

scanning lines arranged substantially in parallel;

signal lines arranged substantially perpendicular to the scanning lines;

pixel electrodes each arranged on a respective patch in a matrix formed by the scanning and signal lines;

a switching element disposed at or around an intersection of one of the scanning lines and one of the signal lines and configured to input a signal to a respective one of the pixel electrodes from said one signal line in accordance with an electric current on said one scanning line;

a storage-capacity-forming extended portion extended from a first one of the pixel electrodes towards a second of one of the pixel electrodes, said first pixel electrode being interposed between first and second ones of the scanning lines and configured to be supplied with a signal in accordance with an applied current on the first scanning line, said second pixel electrode configured to be supplied with a signal in accordance with an applied current on the second scanning line, and said storage-capacity-forming extended portion overlapping the second scanning line with an insulator film therebetween;

a tandem repair circuit comprised of,

a first connector electrode connected with the storage-capacity-forming extended portion extended from the first pixel electrode,

a second connector electrode distanced from the first connector electrode and connected with said second pixel electrode,

a third connector electrode bridging over the first connector electrode to the second connector electrode, and

a contact hole passing through the insulator film and electrically connecting the first connector electrode to the storage-capacity-forming extended portion, said contact hole being placed within contours of said second scanning line[[;]],

said first connector electrode comprising,

a thin-width wiring portion extending from an area above said third connector electrode to an area above said one scanning line and substantially perpendicularly crossing a contour of said one scanning line; and

a thick-width wiring portion connected with an end of said thin-width wiring portion and located within contours of said scanning lines.

Claim 3 (Previously Presented): A matrix array substrate according to claim 2, said thick-width wiring portion having a size along said one scanning line larger than a width of said one scanning line.

Claim 4 (Previously Presented): A matrix array substrate according to claim 3, wherein said size of the thick-width wiring portion is substantially equal to a sum of a size of said contact hole and a margin configured to absorb a deviation of alignment during patterning of said contact hole.

Claim 5 (Canceled).

Claim 6 (Previously Presented): A matrix array substrate according to claim 2, wherein said third connector electrode is included in a first-layer metal pattern and formed simultaneously with the scanning lines, and said first and second connector electrodes are included in a second-layer metal pattern and formed simultaneously with the signal lines.

Claim 7 (Previously Presented): A matrix array substrate according to claim 6, wherein said second-layer metal pattern is formed of aluminum metal or an aluminum alloy.

Claim 8 (Previously Presented): A matrix array substrate according to claim 6, wherein said pixel electrodes and said storage-capacity-forming extended portions are included in a pattern of transparent electric-conductive material disposed in a layer above said first- and second-layer metal patterns.

Claims 9-11 (Canceled).